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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,372	04/22/2004	Hiromichi Waki	TSUT.0032	7100

7590 06/15/2006

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EXAMINER	
DOAN, THERESA T	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/829,372	WAKI ET AL.	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-35* is/are pending in the application.

4a) Of the above claim(s) *13-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/939,738.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 21-35 in the reply filed on 03/29/06 is acknowledged.

Claim Objections

2. Claim 21 is objected to because of the following informalities:

In claim 21, line 9, a phrase "...a lower electrode ..." should be changed to "...a **upper** electrode ...".

In claim 21, line 22, a phrase "...a conductive film being embedded in the plug ..." should be changed to "...a conductive film being embedded in the **contact hole** ...".

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 21-22, 24 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Amanuma (6,188,098) of record.

Regarding claim 21, Amanuma (Fig. 15) discloses a semiconductor integrated circuit device comprising:

(a) an information transfer MISFET including a gate insulating film 4 formed over a semiconductor substrate 1, a gate electrode 5 formed over the gate insulating film 4, and source and drain regions 3 formed in the semiconductor substrate 1 on both sides of the gate electrode 5;

(b) an insulating film 6 formed over the information transfer MISFET;

(c) a capacitor 19 including a lower electrode 8 comprised of a first conductive film, a capacitive insulating film 9 (column 5, lines 56-58) formed over the lower electrode 8 and comprised of a high-dielectric or ferrodielectric material, and a upper electrode 10 comprised of a second conductive film and electrically connected to one of the source and drain regions 3; and

(d) a first shielding film 7 comprised of an insulating film formed under the lower electrode 8 and a second shielding film 12 comprised of an insulating film formed on the upper electrode 10,

wherein the capacitor 19 is covered with the first 7 and second shielding films 12, the capacitor 19 is formed over the source or drain region 3 of the information transfer MISFET through the insulating film 6,

the first shielding film 7 and second shielding film 12 are formed over the source and drain regions 3 of the information transfer MISFET, and

a plug 15 is formed in a contact hole formed by removing the insulating film 6 and the first shielding film 7 located on another of the source and drain regions 3 of the

information transfer MISFET, with a conductive film being embedded in the contact hole, and is connected to the lower electrode 8 (See Figs. 1 and 15). It is note that the process limitation (formed by removing) would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 22, Amanuma (Fig. 15) discloses the first shielding film 7 is formed by a pattern larger than that of the lower electrode 8, and the second shielding film 12 is formed so as to cover an upper surface and a sidewall of the upper electrode 10, a sidewall of said capacitive insulating film 9, and a sidewall of the lower electrode 8 by being connected to said first shielding film outside the lower electrode.

Regarding claim 24, Amanuma (Fig. 15) discloses the second shielding film 12 is formed by a pattern larger that that of the lower electrode 8, and the first shielding film is formed so as to overlap with the second shielding film 12 outside the lower electrode. It is note that the process limitation (formed by a pattern) would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 27, Amanuma (Fig. 15) discloses an interlayer insulating film 13 having barrier layers on the information transfer MISFET and capacitor 19 is formed, and a wiring 14 is formed on the interlayer insulating film 13.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 21-35 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-5 of U.S. Patent No. 6,509,597 in view of Amanuma (6,188,098).

Although the conflicting claims are not identical, they are claiming common subject matter, as follows: both U.S. Patent and instant application claimed a semiconductor integrated circuit device having an information transfer MISFET. Specifically, regarding claim 21 of instant application discloses a semiconductor integrated circuit device (claim 1, line 1) comprising: an information transfer MISFET including a gate insulating film formed over a semiconductor substrate, a gate electrode formed over the gate insulating film, and source and drain regions formed in the semiconductor substrate on both sides of the gate electrode (claim 1, lines 6-11); a capacitor including a lower electrode comprised of a first conductive film, a capacitive insulating film formed over the lower electrode and comprised of a high-dielectric or

ferrodielectric material, and a upper electrode comprised of a second conductive film and electrically connected to one of the source and drain regions (claim 1, lines 12-18); and a first shielding film comprised of an insulating film formed under the lower electrode and a second shielding film comprised of an insulating film formed on the upper electrode, wherein the capacitor is covered with the first and second shielding films (claim 1, lines 19-21).

The U.S. Patent No. 6,509,597 does not claim a conductive plug connected to the lower electrode of the capacitor.

However, Amanuma (Fig. 15) teaches a conductive plug 15 is formed in a contact hole connected to the lower electrode 8 and the first shielding film 7 located on the source and drain regions 3 of the information transfer MISFET. Accordingly, it would have been obvious to form the conductive plug connected to the lower electrode of the capacitor in order to make the electrical contacts to the source/drain of transistor, as taught by Amanuma.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Theresa Doan
June 9, 2006.